## *Amendments to the Specification*

Please make the following amendments to the Specification:

Page 1, lines 5-11

Two commonly assigned patent applications in the name Mark Taunton, ~~filed on the same date as the present application,~~ each also entitled "Multi-tone transmission", and with ~~reference numbers BP1755~~ Application Nos. 09/921,758, filed August 6, 2001 and ~~BP1757~~ 09/921,757, filed August 6, 2001, are incorporated herein by reference.

Page 16, lines 4-14

The symbols are then passed to both a symbol buffer 158 and also passed to an AFE preprocessing model 32. The symbols are output through analogue front end 146. Although the symbol buffer 158 is shown as being separate from the modulator 126, in embodiments the buffer is incorporated in the modulator. The term analogue front end, as used in the present specification, is not necessarily intended to refer to a purely analogue device. Indeed, the preprocessing is often carried out in the digital domain. The term 'analogue front end' does however include the digital-to-analog converter (DAC) and associated circuitry which supplies the analogue output signal, typically via an amplifier (line-driver), to the communication path carrying the final transmitted signal.

Page 16, lines 20-27

If the peak amplitude in a given symbol exceeds a predetermined threshold, then control signals 162 indicated as dashed lines are output to cause the symbol to be regenerated. Intermediate data 18 input into one of the intermediate stages is amended, or regenerated, in such a way that the regenerated data still corresponds to the original input data, by changing one or more bits in the intermediate data. The regenerated intermediate data is then processed through subsequent intermediate stages 14, 16, and the Fourier transform module ~~26~~ <u>24</u> to produce a regenerated symbol.

Page 17, lines 20-24

By modelling ~~162~~ the subsequent processing in the analogue front end 146 in model 2, it is possible to determine when a symbol needs to be regenerated even in the presence of processing in the analogue front end 146. Thus, the crest factor of the data stream output from the analogue front end may be reduced.

Page 18, lines 6-18

In the embodiment described, the ~~step~~ <u>preprocessing stage</u> 14 following the introduction of regenerated intermediate data 18 is a scrambling ~~step~~ <u>stage</u>. ~~Such a step~~ <u>Scrambling</u> has a particularly strong effect: any single bit change (0 to 1 or 1 to 0) in the payload of the ATM cell stream will have a permanent effect on the subsequent output from the payload scrambler (after an initial period while data bits percolate through its internal memory), since that process has local feedback and retains a memory of the effect of all bits which have passed through. ~~The~~ <u>A</u> second scrambling ~~step~~ <u>stage</u>,

applied to the full data stream (including ATM cell headers and other overhead data), similarly causes all later data output values (beyond an initial short sequence) to be affected as a result of changing a single input bit.

It is however not necessary that the subsequent ~~step~~ stage is a scrambling ~~step~~ stage. The scrambling ~~step~~ can be carried out later or not at all.

Page 19, lines 9-16

A second embodiment will now be described, specifically with reference to an ADSL ~~system~~ flow diagram. Figure 2 shows a flow diagram of an ADSL modem that transmits ATM cells 102. In a ~~first~~ fast data path 100, the cells are buffered 104, and idle cells 106 are inserted 108 as required. The cell payload is then scrambled 110, and a cyclic redundancy check 112 performed. Data bytes from the ATM cell stream are then grouped together by framing 114, adding fast bytes 116 where required. Scrambling 118 then takes place, followed optionally by Reed-Solomon forward error correction 120.

Page 20, lines 18-21

The AFE preprocessing ~~model~~ step 162 models the effect on the symbol of the AFE preprocessing, including the oversampling and any filtering. Since the AFE preprocessing is generally carried out in the digital domain, the skilled person will not have any difficulty in modelling the preprocessing.

Page 21, lines 17-28

Note that each ~~functional block~~ step shown in the Figure 2 within the Data Path modules, the Modulator module and the Regenerator Control module, could in principle be implemented either by hardware or by software, or by some combination of the two. The AFE module steps normally ~~uses~~ use hardware blocks for its functions.

The preprocessing ~~model~~ step 162 may be implemented in various ways: (a) as a fixed hardware block, matched in function to the preprocessing block in the AFE; (b) as a programmable hardware block (for example, having variable coefficients in its filters, and/or switchable processing elements) or (c) purely as a software program to be run on the central processor of the modulator. In the latter two cases, the preprocessing model used can be varied through software so as to adapt it for use with different analogue front ends.

Page 23, lines 20-32

In the embodiment, the preprocessing and DAC units of the AFE 146 are implemented in one chip 151 and the modulator 126 including the model ~~162~~ 32 and buffer 158 in another chip 153; the line-driver 150 is a third separate device.

The digital modulator 126 is built on a small geometry, more expensive process, so as to keep its size down and maximise digital processing speed. The preprocessing and DAC units of the AFE ~~46~~ 146 are built on a larger-geometry, but cheaper and slower silicon process, which makes the design of analogue elements easier, and reduces the chip's cost.

The modelling ~~unit~~ step 162 in the modulator, in this example, is chosen to be another instance of the preprocessing unit 160 in the AFE 146. However, because of the smaller geometry, it takes up less space. Since it is on the faster modulator chip 126, it can be clocked much faster.

Page 24, lines 1-10

Further, practical implementations of the invention may include multiple output channels. Since digital logic (including the preprocessing unit 160) in the AFE 146 is generally clocked more slowly than the modulator 126, and for other reasons, one physical copy of the preprocessing circuitry 160 is then used in the AFE for each output channel supported, rather than multiplexing the circuitry across different channels. However, in the modulator 126, the faster clock speed allows the modelling circuitry ~~162~~ 32 to be time division multiplexed across multiple channels, thereby saving sapce. Thus, the overhead associated with the duplication of the preprocessing circuitry 160 as the modelling unit ~~162~~ 32 may be less than would at first be thought.

Page 27, line 23 to page 28, line 3

This observation provides another method of changing the data stream, for symbols where it is desired to re-generate because of a peak above the specified threshold in the encoded time-domain version of the symbol. What can be done is to check whether any bite of data carried by the symbol is part of the payload of an idle cell, and if so, to make a modification in that byte. Because the payload of idle cells is ignored by the receiver 200, any bit of the 8 in the byte can be modified, allowing up to

255 possible modifications (relative to the original value) to be tried out--this is far more than enough! In general, to achieve maximum effect, the earliest available idle-cell payload byte in the data for the symbol should be so modified, since all modifications affect (by spreading) only the encoded form of alter bytes in the stream (and hence, that portion of the stream which is carried in the rest of the symbol).

Page 28, lines 15-28

One proviso to this method is that one way of checking the error rate on an ADSL link, sometimes employed for purposes of link maintenance and management, is for the receiving modem 200 to examine the payload bytes of idle cells before it discards them, comparing each byte against the fixed value it is defined to hold in any idle cell. Any errors found in the comparison are assumed to have arisen as a result of uncorrected errors in transmission of the data stream over the ADSL link. Some modems keep count of the error rate on this basis (measured as a moving average of the number of bits in idle cells which are found to be incorrect, divided by the total number of bits in the idle cells seen, over some measurement interval). In such cases, the deliberate introduction of changes to idle cell payload bytes will give rise to an incorrect assessment of the true error rate by the receiving modem 200. In the worst case this may trigger an attempt to re-configure or re-initiate the link, so as to maintain the apparent error rate below the required maximum level.